What is claimed is:

1. A lead frame for use in a chip package, comprising:

a. a central region having a first plurality of sides;

b. a peripheral edge region having a second plurality of sides positioned in spaced relation around said central region;

c. a first set of leads extending from each of said second plurality of sides, each of said first set of leads being partially defined by a first terminal end, first opposing side surfaces each of which extends along a respective first longitudinal axis, and a lower surface that extends in a first plane;

d. a second set of leads extending from said second plurality of sides, each of said second set of leads being partially defined by a second terminal end, second opposing side surfaces each of which extends along a respective second longitudinal axis, and an upper surface that extends in a second plane; and

e. wherein each of said first set of leads are positioned in staggered relation to corresponding ones of said second set of leads such that said first terminal ends are spaced from said second terminal ends by a first predetermined distance, each of said first longitudinal axes are substantially parallel to and spaced from the adjacent ones of said second longitudinal axes by a second predetermined distance, and said first plane is spaced from said second plane by a third predetermined distance.

2. The lead frame according to claim 1, wherein said first set of leads are formed by a mask having resist material arranged to define the pattern of said first set of leads.

3. The lead frame according to claim 1, wherein said second set of leads are formed by a first mask having resist material arranged to define the pattern of said second set of leads.

4. The lead frame according to claim 3, wherein said first set of leads are formed by a second mask having resist material arranged to define the pattern of said first set of leads, said first and second masks being asymmetrical with respect to one another.

5. A method for forming a chip package, comprising the steps of:

a. providing a lead frame of predetermined thickness having an upwardly facing surface and a downwardly facing surface, a central region having a first plurality of sides, and a peripheral edge region having a second plurality of sides extending around and spaced from said first plurality of sides;

b. providing an upper mask to position resist material on said upwardly facing surface that define a first set of leads extending from each of said second plurality of sides, each of said first set of leads being partially defined by a first terminal end, first opposing side surfaces each of which extends along a respective first longitudinal axis, and a lower surface that extends in a first plane;

c. providing a lower mask to position resist material on said downwardly facing surface that define a second set of leads extending from said second plurality of sides, each of said second set of leads being partially defined by a second terminal end, second opposing side surfaces each of which extends along a respective second

longitudinal axis, and an upper surface that extends in a second plane, and a portion of said second set of leads that are vertically aligned with a portion of said first set of leads;

d. etching away portions of said upwardly facing surface that are not covered with said resist material to a depth greater than one half of said predetermined thickness; and

e. etching away portions of said downwardly facing surface that are not covered with said resist material to a depth greater than one half of said predetermined thickness, wherein each of said first set of leads are positioned in staggered relation to corresponding ones of said second set of leads such that said first terminal ends are spaced from said second terminal ends by a first predetermined distance, each of said first longitudinal axes are substantially parallel to and spaced from the adjacent ones of said second longitudinal axes by a second predetermined distance, and said first plane is spaced from said second plane by a third predetermined distance.

6. The method according to claim 5, comprising the further step of encapsulating said chip carrier package in a resin.

7. The method according to claim 6, comprising the further step of removing said peripheral edge.

8. The method according to claim 7, wherein said step of removing said peripheral edge is by saw singulation.

9. A chip package, comprising:

a. a first set of leads each of which is partially defined by a first terminal end, first opposing side surfaces each of which extends along a respective first longitudinal axis, and a lower surface that extends in a first plane;

b. a second set of leads each of which is partially defined by a second terminal end, second opposing side surfaces each of which extends along a respective second longitudinal axis, and an upper surface that extends in a second plane; and

c. wherein each of said first set of leads are positioned in staggered relation to corresponding ones of said second set of leads such that said first terminal ends are spaced from said second terminal ends by a first predetermined distance, each of said first longitudinal axes are substantially parallel to and spaced from the adjacent ones of said second longitudinal axes by a second predetermined distance, and said first plane is spaced from said second plane by a third predetermined distance.

10. The chip package of claim 9, further comprising a die pad positioned in spaced relation to said first and second sets of leads.

11. The chip package according to claim 10, further comprising a chip having a predetermined number of input/outputs and mounted on said die pad.

12. The chip package according to claim 11, further comprising wire bonds interconnecting said input/outputs of said chip to corresponding ones of said first and second sets of leads.

13. The chip package according to claim 12, further comprising an epoxy resin encapsulating said package leaving a portion of said first and second sets of leads exposed.